University of California, Santa Barbara

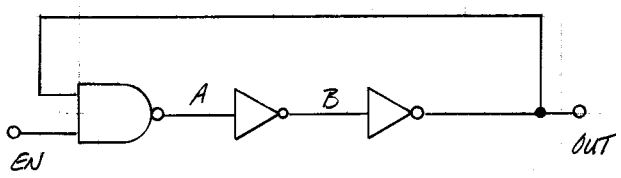
Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Homework #3

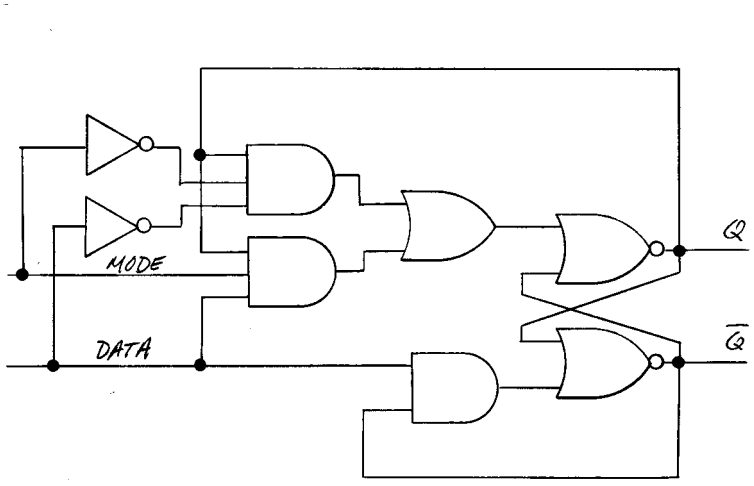
Problem #1.

Construct a timing diagram for the circuit shown below. Make the following assumptions: OUT is initially 1; the EN signal is low for the first 10 ns then goes high forever; all gate delays are 10 ns. Show the EN, A, B and OUT signals as a function of time for 70 ns.



Problem #2.

For the latch shown below,



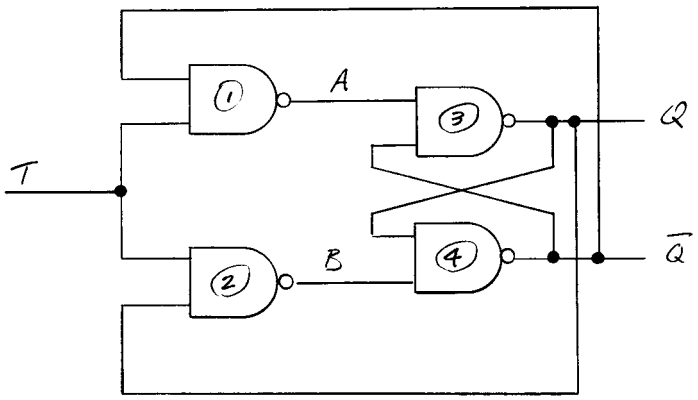
Determine the following:

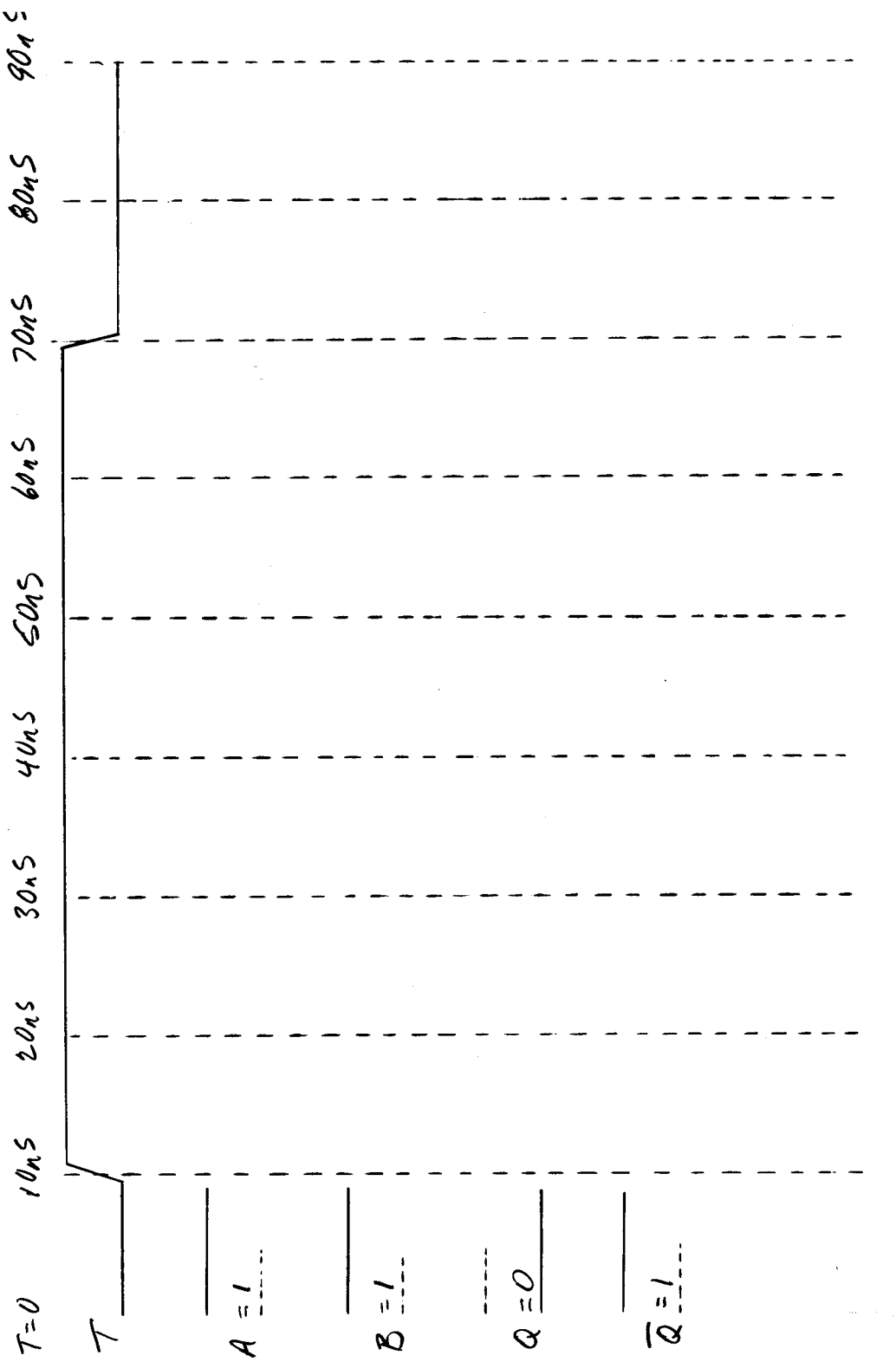
1. Characteristic Table
2. Characteristic Equation
3. State Diagram
4. State Table

Problem #3.

Complete the timing diagram (on the following page) for the logic diagram shown below. Assume the propagation delay for gates 1 and 2 is 10 ns and the propagation delay for gates 3 and 4 is 5 ns (both low to high and high to low transitions, t_{PLH} and t_{PHL}).

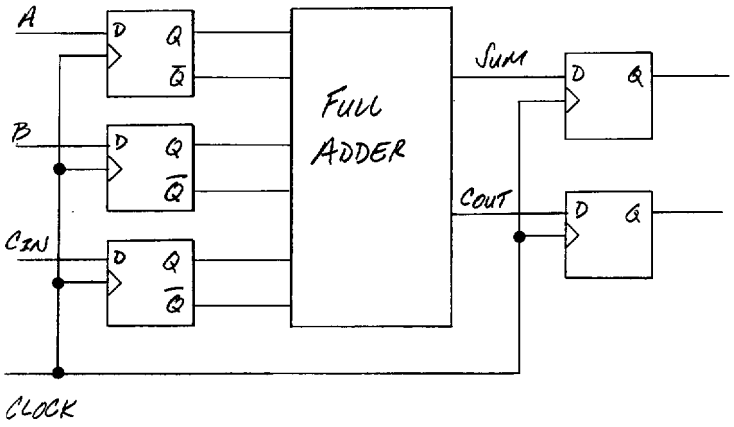
Include arrows on your timing diagram indicating the sequence and interdependence of signal transitions. Your answer is incomplete without this annotation.




T=0
10nS
20nS
30nS
40nS
50nS
60nS
70nS
80nS
90nS
T
A = 1
B = 1
Q = 0
$\overline{Q}$ = 1

Problem #4.

The block diagram below shows a portion of a digital system consisting of three input flip flops, a combinational full adder circuit and two output flip flops.



The sum and carry out networks can be realized in two level sum of products representation and can be implemented with either AND and OR gates, or with NAND gates alone. In either case inverters aren't necessary since the input D flip flops provide both the true and complemented versions of A, B and Cin.

The gates and D flip flops have the following timing parameters (all in nS):

	t_{PLH}	t_{PHL}	
NAND Gate	22	15	
AND Gate	27	19	
OR Gate	15	22	
	$t_{CLK\ to\ Q}$	t_{setup}	t_{hold}
D Flip Flop	40	20	5

Determine the minimum clock period if:

(1) the implementation is done with AND and OR gates

(2) the implementation is done with only NAND gates

Be sure to consider both high to low and low to high transitions in both the sum and carry out networks in determining the delay through the adder.

Problem #5.

Design a 3-bit gray code counter using negative edge triggered D flip flops. The counter should increment on each clock cycle. In your answer, include (1) a state diagram, (2) a state table, (3) a next state map and (4) all Kmaps used in determining flip flop inputs.

Problem #6.

Complete the timing diagram for the master-slave flip flop shown below. You can assume the values of QS and QnS are initially 0 and 1, respectively. Use arrows to indicate the sequence of signal transitions.